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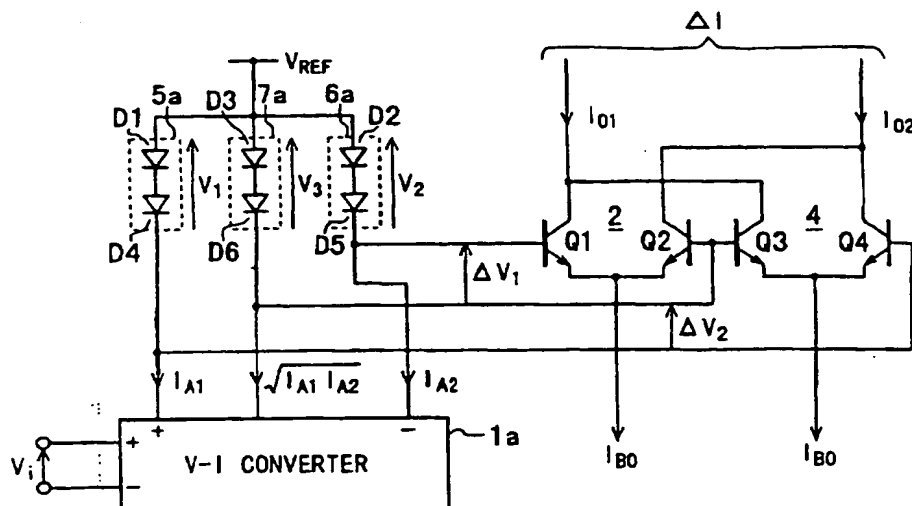
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(54) Abstract Title

Bipolar OTA based on hyperbolic function transformation

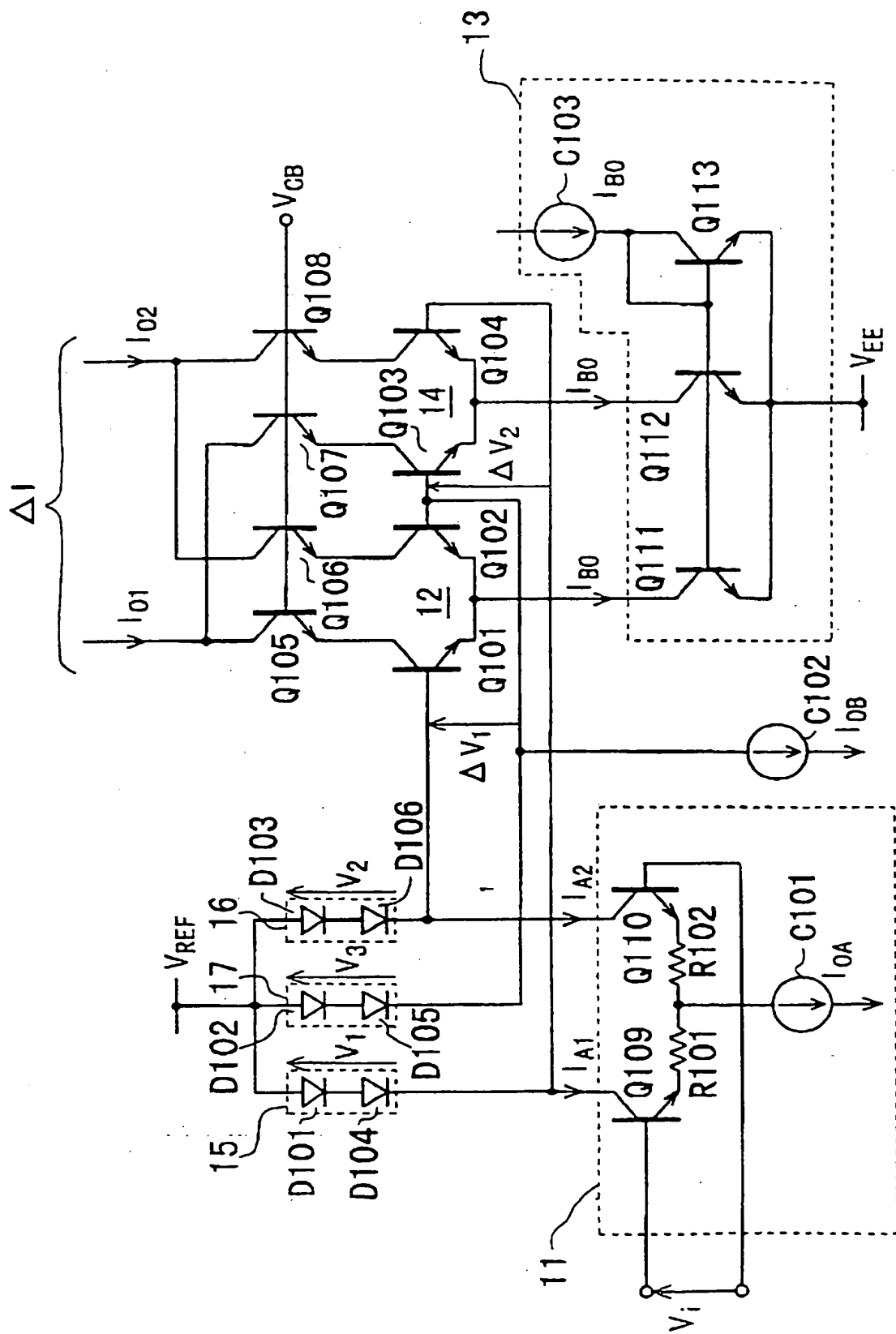
(57) An OTA having a completely linear transconductance is provided. This OTA is comprised of a V-I converter 1a, a first I-V converter 5a, a second I-V in converter 6a, a third I-V converter 7a, a first differential pair 2 of first and second emitter-coupled bipolar transistors driven by a first constant current, and a second differential pair 4 of third and fourth emitter-coupled bipolar transistors driven by a second constant current. The V-I converter converts a differential input voltage to first and second output currents linearly related to the differential input voltage and generates a third output current. The first I-V converter converts the first output current to a first output voltage to be applied to a base of the fourth transistor. The second I-V converter converts the second output current to a second output voltage to be applied to a base of the first transistor. The third I-V converter converts the third output current to a third output voltage to be applied to bases of the second and third transistors. The third output voltage is equal to a middle point voltage (i.e., a half) of a sum of the first and second output voltages. Other embodiments (figures 3, 4 and 5) show the third output voltage derived from third and fourth currents from the V-I converter and the use of a quadritail cell (8) (fig 5).

FIG. 2



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FIG. 1
PRIOR ART



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FIG. 3

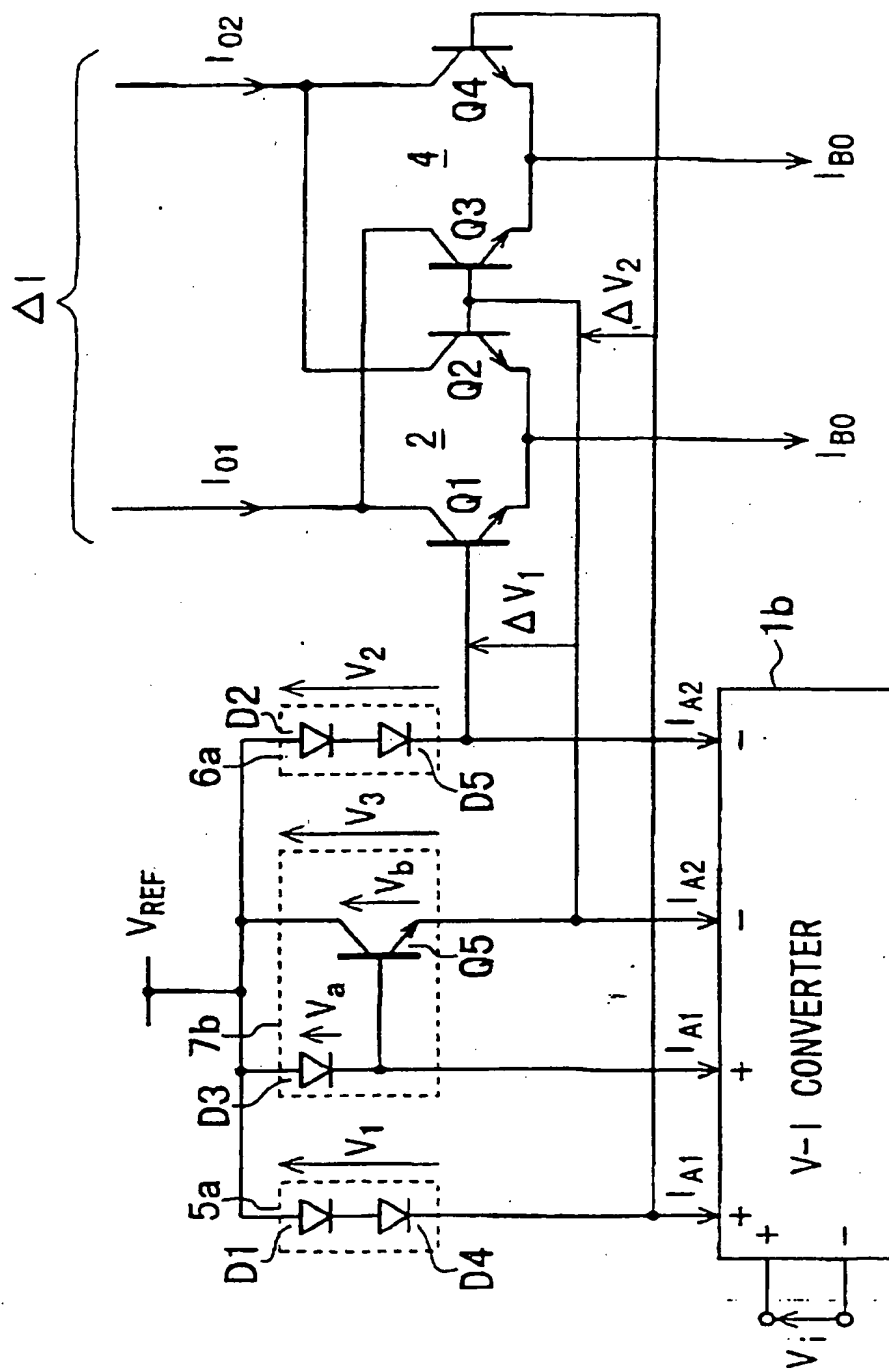


FIG. 4

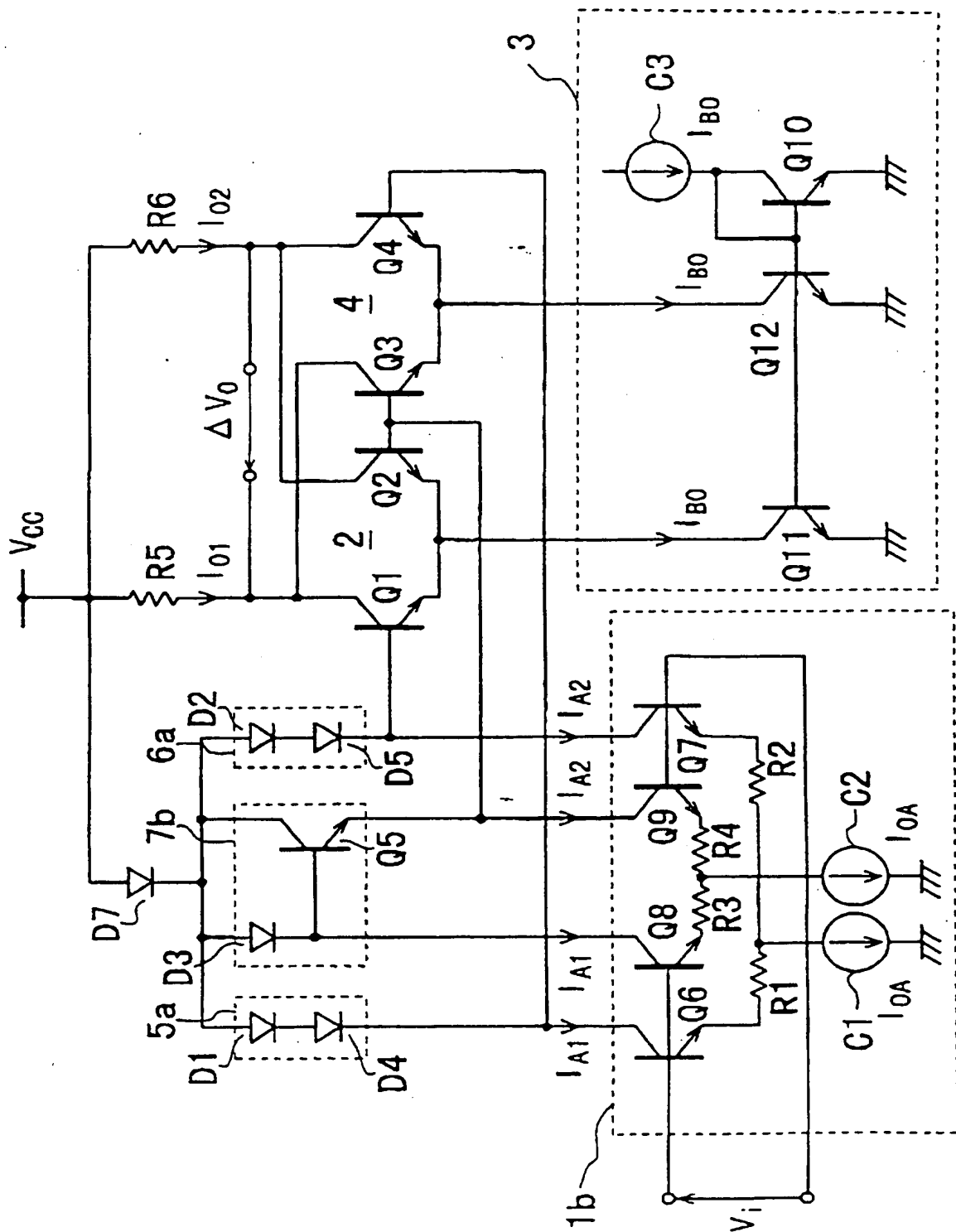
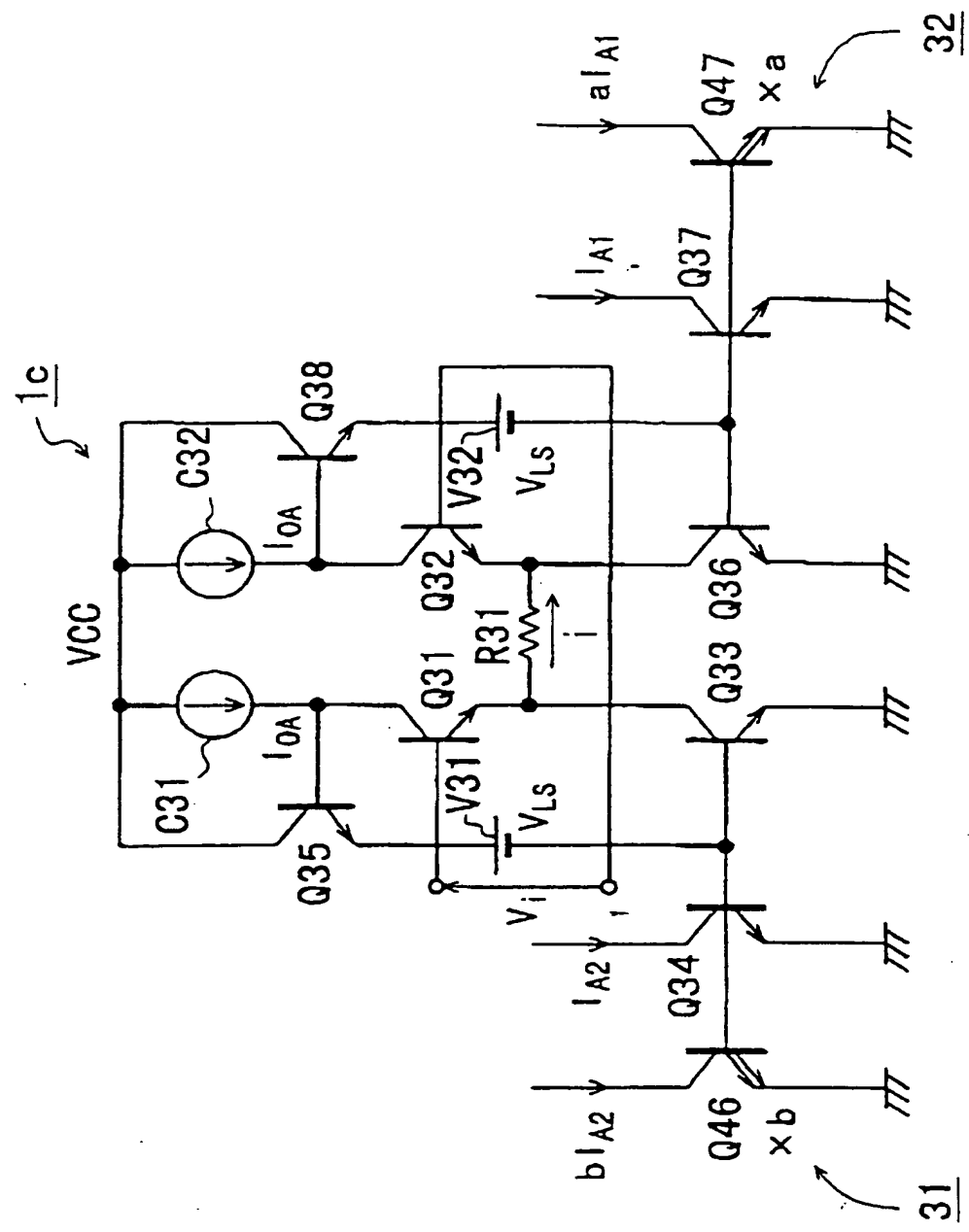
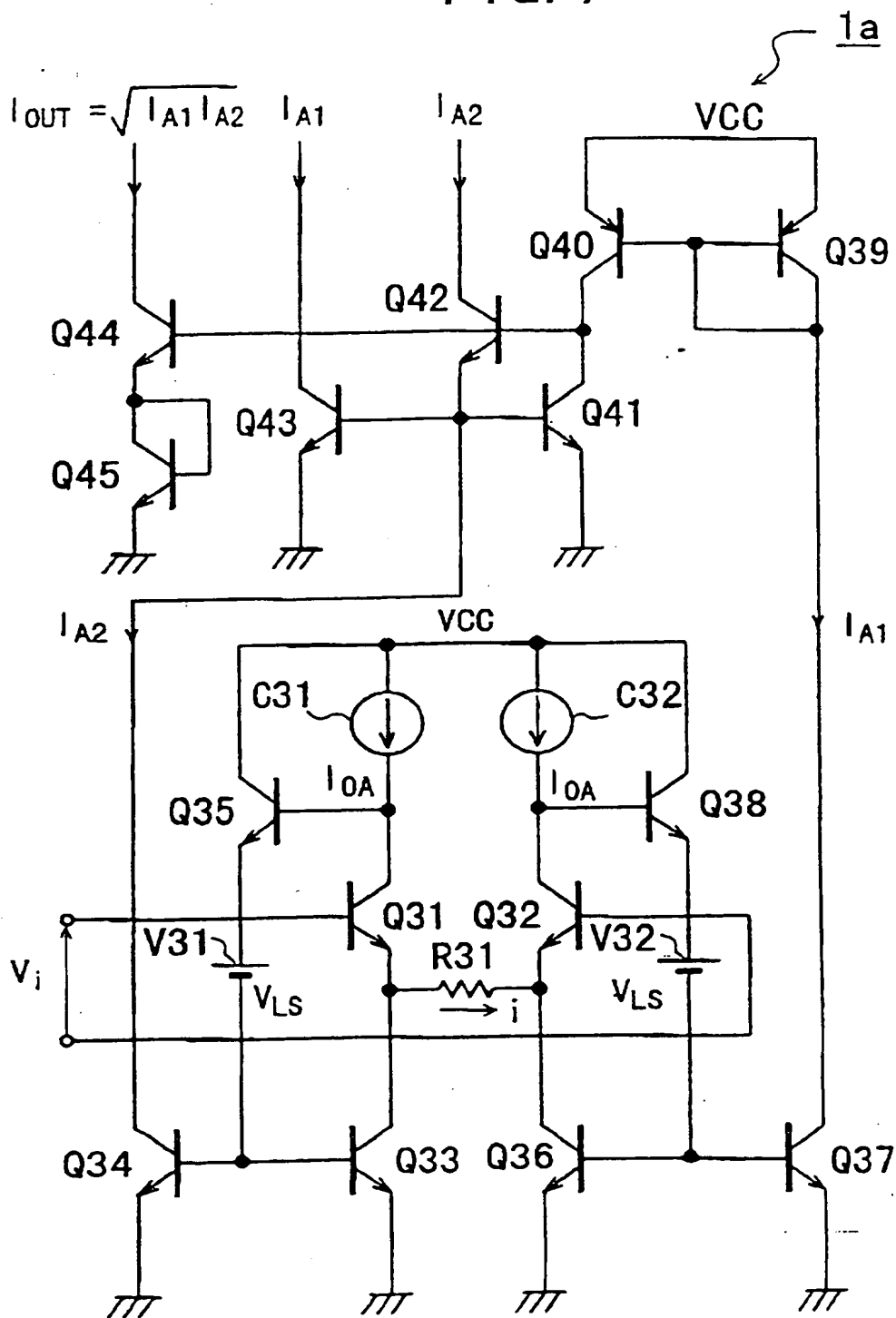


FIG. 6



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FIG. 7



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BIPOLAR OTA

BASED ON \tanh^{-1} - \tanh TRANSFORMATION

BACKGROUND OF THE INVENTION

5 1. Field of the Invention

The present invention relates to an operational transconductance amplifier and more particularly, to a bipolar operational transconductance amplifier having a completely linear transconductance and suitable for a semiconductor integrated circuit (IC), which is based on the
10 inverse hyperbolic tangent-hyperbolic tangent transformation.

2. Description of the Prior Art

A differential amplifier circuit having a superior transconductance linearity within a comparatively wide input
15 voltage range has been known as an "Operational Transconductance Amplifier (OTA)". Therefore, the OTA may be termed a "translinear" circuit.

A conventional bipolar translinear multiplier is shown in Fig. 1, which is disclosed in the Japanese Patent No.
20 2,512,385 issued in April 1996 and which corresponds to the US patent No. 5,331,289 issued in July 1994. This multiplier has substantially a same configuration as an OTA.

As shown in Fig. 1, a differential pair of emitter-coupled, npn-type bipolar transistors Q109 and Q110 driven by

a constant current sink C101 (current: I_{0A}) constitute a voltage-to-current (V-I) converter 11. The transistors Q109 and Q110 have emitter resistors R101 and R102, respectively. Bases of the transistors Q109 and Q110 constitute a pair of
5 input terminals of the V-I converter 11, and they are applied with a differential input voltage V_1 . Collectors of the transistors Q109 and Q110 constitute a pair of output terminals of the V-I converter 11.

An end of a diode pair 15 of serially connected
10 diodes D101 and D104 is connected to the collector of the transistor Q109. Another end of the diode pair 15 is connected to a reference voltage line applied with a reference voltage V_{REF} . An end of a diode pair 16 of serially connected diodes D103 and D106 is connected to the collector
15 of the transistor Q110. Another end of the diode pair 16 is connected to the reference voltage line applied with the reference voltage V_{REF} .

Further, a diode pair 17 of serially connected diodes D102 and D105 is additionally provided. An end of the diode
20 pair 17 is connected to a constant current sink C102 (current: I_{0B}). Another end of the diode pair 17 is connected to the reference voltage line applied with the reference voltage V_{REF} .

A differential pair 12 of emitter-coupled, npn-type

bipolar transistors Q101 and Q102 is driven by a current I_{B0} produced by a current mirror circuit 13. Bases of the transistors Q101 and Q102, which constitute a pair of input terminals of the differential pair 12, are respectively
5 connected to the collector of the transistor Q110 and the diode pair 17. The bases of the transistors Q101 and Q102 are applied with a differential input voltage ΔV_1 . Collectors of the transistors Q101 and Q102, which constitute a pair of output terminals of the differential pair 12, are connected
10 to emitters of npn-type bipolar transistors Q105 and Q106, respectively.

A differential pair 14 of emitter-coupled, npn-type bipolar transistors Q103 and Q104 is driven by a current I_{B0} produced by the current mirror circuit 13. Bases of the
15 transistors Q103 and Q104, which constitute a pair of input terminals of the differential pair 14, are respectively connected to the diode pair 17 and the collector of the transistor Q109. The bases of the transistors Q103 and Q104 are applied with a differential input voltage ΔV_2 . Collectors
20 of the transistors Q103 and Q104, which constitute a pair of output terminals of the differential pair 14, are connected to emitters of npn-type bipolar transistors Q107 and Q108, respectively.

Bases of the transistors Q105, Q106, Q107 and Q108 are connected in common to be applied with a voltage V_{CB} . Collectors of the transistors Q105 and Q107 are coupled together to constitute a first output terminal of the translinear multiplier. Collectors of the transistors Q106 and Q108 are coupled together to constitute a second output terminal of the translinear multiplier.

The current mirror circuit 13 is comprised of npn-type bipolar transistors Q111, Q112, and Q113 whose emitters are connected in common to a voltage line applied with a power supply voltage V_{BB} , and a current source C103 supplying an input current I_{B0} . Bases of the transistors Q111, Q112, and Q113 are coupled together. The bases of the transistors Q111 and Q112 are connected to the coupled emitters of the transistors Q101 and Q102 and the coupled emitters of the transistors Q103 and Q104, respectively. The base and a collector of the transistor Q113 are coupled together to be connected to the current source C103.

Next, the operation principle of the conventional translinear multiplier shown in Fig. 1 is explained below.

Supposing that the base-width modulation (i.e., the Early voltage) is ignored and that the dc common-base current gain factor of a bipolar transistor is equal to unity, a collector current I_c of a bipolar transistor is typically

given as the following expression (1).

$$I_C = I_S \left\{ \exp \left(\frac{V_{BE}}{V_T} \right) - 1 \right\} \quad (1)$$

5 In the expression (1), V_{BE} is a base-to-emitter voltage of a bipolar transistor, and I_S is the saturation current thereof. Also, V_T is the thermal voltage defined as $V_T = kT/q$, where k is the Boltzmann's constant, T is absolute temperature in degrees Kelvin, and q is the charge of an
10 electron.

 When a bipolar transistor is normally operating and the base-to-emitter voltage V_{BE} is equal to approximately 600 mV, the exponential part $\exp(V_{BE}/V_T)$ in the expression (1) has a value approximately equal to e^{10} . Therefore, the constant
15 part "-1" can be ignored.

 Thus, the above expression (1) can be approximate to the following.

$$I_C = I_S \exp \left(\frac{V_{BE}}{V_T} \right) \quad (1')$$

20

 The equation (1') can be rewritten to the following equation (2).

$$V_{BE} = V_T \ln \left(\frac{I_C}{I_S} \right) \quad (2)$$

The V-I converter 11 outputs a pair of differential
 5 output currents I_{A1} and I_{A2} at the collectors of the
 transistors Q109 and Q110 according to the differential input
 voltage V_i , respectively.

Supposing that the V-I converter 11 has a linear
 transfer characteristic, each of the differential output
 10 currents I_{A1} and I_{A2} can be expressed as the sum of the
 constant current ($I_{OA}/2$) that flows the corresponding output
 terminal of the converter 11 (i.e., the collector of the
 transistor Q109 or Q110) and a variable current ($G_m V_i/2$)
 proportional to the applied differential input voltage V_i ,
 15 where ($G_m/2$) is the transconductance of the converter 11.

Therefore, the differential output currents I_{A1} and
 I_{A2} of the converter 11 are given by the following equations
 (3) and (4), respectively,

$$I_{A1} = \frac{1}{2} (I_{OA} + G_m V_i) \quad (3)$$

$$I_{A2} = \frac{1}{2} (I_{OA} - G_m V_i) \quad (4)$$

Generally, the forward voltage drop of a diode is equal to the base-to-emitter voltage of a bipolar transistor. Therefore, the base-to-emitter voltage V_{BE} in the above equation (2) may be rewritten to the voltage drop of each of the diodes D1, D2, D3, D4, D5, and D6. On the other hand, the differential output currents I_{A1} and I_{A2} flow through the diode pairs 15 and 16, respectively. The constant current I_{OB} flows through the diode pair 17.

Accordingly, the voltage drops V_1 , V_2 , and V_3 of the diode pairs 15, 16, and 17 are expressed as the following equations (5), (6), and (7), respectively.

$$V_1 = 2 V_T \ln \left(\frac{I_{A1}}{I_S} \right) = 2 V_T \ln \left(\frac{I_{OA} + G_m V_i}{2 I_S} \right) \quad (5)$$

$$V_2 = 2 V_T \ln \left(\frac{I_{A2}}{I_S} \right) = 2 V_T \ln \left(\frac{I_{OA} - G_m V_i}{2 I_S} \right) \quad (6)$$

$$V_3 = 2 V_T \ln \left(\frac{I_{OB}}{I_S} \right) \quad (7)$$

Accordingly, using the above equations (5), (6), and (7), the differential input voltages ΔV_1 and ΔV_2 of the differential pairs 12 and 14 are given by the following

equations (8) and (9), respectively.

$$\Delta V_1 = V_2 - V_3 = 2 V_T \ln \left(\frac{I_{OA} - G_m V_i}{2 I_{OB}} \right) \quad (8)$$

$$\Delta V_2 = V_3 - V_1 = 2 V_T \ln \left(\frac{2 I_{OB}}{I_{OA} + G_m V_i} \right) \neq \Delta V_1 \quad (9)$$

5

As clearly seen from the equations (8) and (9) that the differential input voltages ΔV_1 and ΔV_2 are not equal. This means that the voltage V_3 is not equal to the middle point voltage (or, a half) of the sum of the voltages V_1 and V_2 ; i.e.,

$$V_3 \neq (1/2) (V_1 + V_2).$$

It is well known that the differential output current ΔI ($= I_{O1} - I_{O2}$) of the cross-coupled differential pairs 12 and 14, which are driven by the constant currents I_{B0} and which are respectively applied with the differential input voltages ΔV_1 and ΔV_2 , is expressed as the following expression (10a).

$$\Delta I = I_{O1} - I_{O2} = I_{B0} \left\{ \tanh \left(\frac{\Delta V_1}{2 V_T} \right) + \tanh \left(\frac{\Delta V_2}{2 V_T} \right) \right\} \quad (10a)$$

Substituting the above equations (8) and (9) into the equation (10a) gives the following equation (10b).

$$\begin{aligned} \Delta I &= I_{BO} \left[\tanh \left\{ \ln \left(\frac{I_{OA} - G_m V_i}{2 I_{OB}} \right) \right\} + \tanh \left\{ \ln \left(\frac{2 I_{OB}}{I_{OA} + G_m V_i} \right) \right\} \right] \\ &= I_{BO} \left[\frac{\sinh \left\{ \ln \left(\frac{I_{OA} - G_m V_i}{2 I_{OB}} \right) \right\}}{\cosh \left\{ \ln \left(\frac{I_{OA} - G_m V_i}{2 I_{OB}} \right) \right\}} + \frac{\sinh \left\{ \ln \left(\frac{2 I_{OB}}{I_{OA} + G_m V_i} \right) \right\}}{\cosh \left\{ \ln \left(\frac{2 I_{OB}}{I_{OA} + G_m V_i} \right) \right\}} \right] \end{aligned} \quad (10b)$$

If the hyperbolic-sine (sinh) and hyperbolic-cosine (cosh) functions in the equation (10b) are eliminated by using the known identities, the equation (10b) can be rewritten to the following equation (11).

$$\begin{aligned} \Delta I &= I_{BO} \left[\frac{(I_{OA} - G_m V_i)^2 - 4 I_{OB}^2}{(I_{OA} - G_m V_i)^2 + 4 I_{OB}^2} + \frac{4 I_{OB}^2 - (I_{OA} + G_m V_i)^2}{(I_{OA} + G_m V_i)^2 + 4 I_{OB}^2} \right] \\ &= I_{BO} \left\{ \frac{I_{OA}^2 - (G_m V_i)^2 - 4 I_{OB}^2 - 2 I_{OA} G_m V_i}{I_{OA}^2 - (G_m V_i)^2 + 4 I_{OB}^2 - 2 I_{OA} G_m V_i} \right. \\ &\quad \left. + \frac{4 I_{OB}^2 - I_{OA}^2 - (G_m V_i)^2 - 2 I_{OA} G_m V_i}{I_{OA}^2 + (G_m V_i)^2 + 4 I_{OB}^2 + 2 I_{OA} G_m V_i} \right\} \end{aligned} \quad (11)$$

$$= -32 I_{OA} I_{BO}^3 \left[\frac{G_m V_i}{(I_{OA}^2 + G_m^2 V_i^2 + 4 I_{OB}^2)^2 - 4 I_{OA}^2 G_m^2 V_i^2} \right]$$

The following facts are derived from the above equation (11).

5 First, when the current I_{BO} of the current source C103 is used as another input in addition to the differential input voltage V_i , the circuit configuration shown in Fig. 1 may serve as an analog multiplier. However, it is clear that the differential output current ΔI is not accurately
10 proportional to the product $(V_i \cdot I_{BO})$ of the differential input voltage V_i and the input current I_{BO} .

Second, when the current I_{BO} of the current source C103 is set as a constant value, the circuit configuration shown in Fig. 1 may serve as an OTA. However, it is clear
15 that the differential output current ΔI is not accurately proportional to the differential input voltage V_i .

An OTA and an analog multiplier are essential, basic function blocks in analog signal applications. The OTA is required to have a completely linear transconductance. The
20 multiplier is required to have a complete multiplier characteristic.

However, the conventional multiplier shown in Fig. 1 does not have a complete multiplier characteristic. If this multiplier is used as an OTA, it does not have a complete linear transconductance.

5

SUMMARY OF THE INVENTION

Accordingly, an object of at least the preferred embodiments of the present invention is to provide an OTA having a completely linear transconductance.

Another such object is to provide
10 an OTA that can be used as a translinear multiplier.

The above objects together with others not specifically mentioned will become clear to those skilled in the art from the following description.

An OTA according to a first aspect of the present
15 invention is comprised of a V-I converter, a first current-to-voltage (I-V) converter, a second I-V converter, a third I-V converter, a first differential pair of first and second emitter-coupled bipolar transistors driven by a first constant current, and a second differential pair of third and
20 fourth emitter-coupled bipolar transistors driven by a second constant current.

The V-I converter converts a differential input voltage to first and second output currents linearly related to the differential input voltage and generates a third

output current.

The first I-V converter converts the first output current to a first output voltage which is applied to a base of the fourth transistor.

5 The second I-V converter converts the second output current to a second output voltage which is applied to a base of the first transistor.

10 The third I-V converter converts the third output current to a third output voltage which is applied to bases of the second and third transistors. The third output voltage is equal to a middle point voltage (i.e., a half) of a sum of the first and second output voltages.

15 Collectors of the first and third transistors of the first differential pair are coupled together to constitute a first output terminal of the OTA. Collectors of the second and fourth transistors of the second differential pair are coupled together to constitute a second output terminal of the OTA.

20 An output of the OTA is differentially derived from the first and second output terminals.

With the OTA according to the first aspect of the present invention, the V-I converter converts the differential input voltage to the first and second output currents linearly related to the differential input voltage

and generates the third output current.

The first I-V converter converts the first output current to the first output voltage which is applied to the base of the fourth transistor. The second I-V converter
5 converts the second output current to the second output voltage which is applied to the base of the first transistor. The third I-V converter converts the third output current to the third output voltage which is applied to the bases of the second and third transistors. The third output voltage is
10 equal to the middle point voltage (i.e., a half) of the sum of the first and second output voltages.

Therefore, the difference between the second and third output voltages, which is applied to the first differential pair, is always equal to the difference between
15 the first and third output voltages, which is applied to the second differential pair. This means that the output of the OTA is equal to twice as much as an output of one of the first and second differential pairs.

Each of the outputs of the first and second
20 differential pairs is proportional to the hyperbolic-tangent (\tanh) of the applied difference between the second and third output voltages or the first and third output voltages.

Accordingly, the output of the OTA is linearly related to the differential input voltage. In other words,

the OTA according to the present invention has a completely linear transconductance.

Additionally, if the first and second constant currents for driving the first and second differential pairs
5 are set as equal and used as an input current, the OTA according to the first aspect of the present invention can be used as a translinear multiplier for multiplying the differential input voltage and the input current.

In a preferred embodiment of the OTA according to the
10 first aspect of the present invention, the third output current of the third I-V converter is proportional to the square root of the product of the first and second output currents of the V-I converter.

In this case, it is preferred that each of the first,
15 second, and third I-V converters is formed by two serially-connected diodes. Each of the diodes may be formed by a p-n junction diode or a diode-connected bipolar transistor whose base and collector are coupled together.

An OTA according to a second aspect of the present
20 invention is comprised of a V-I converter, a first I-V converter, a second I-V converter, a third I-V converter, a first differential pair of first and second emitter-coupled bipolar transistors driven by a first constant current, and a second differential pair of third and fourth emitter-coupled

bipolar transistors driven by a second constant current.

The V-I converter converts a differential input voltage to first and second output currents linearly related to the differential input voltage.

5 The first I-V converter converts the first output current to a first output voltage which is applied to a base of the fourth transistor.

 The second I-V converter converts the second output current to a second output voltage which is applied to a base
10 of the first transistor.

 The third I-V converter converts the first and second output currents to a third output voltage which is applied to bases of the second and third transistors. The third output voltage is equal to a middle point voltage (i.e., a half) of
15 a sum of the first and second output voltages.

 Collectors of the first and third transistors of the first differential pair are coupled together to constitute a first output terminal of the OTA. Collectors of the second and fourth transistors of the second differential pair are
20 coupled together to constitute a second output terminal of the OTA.

 An output of the OTA is differentially derived from the first and second output terminals.

With the OTA according to the second aspect of the present invention, because the configuration of the third I-V converter alone is different from that of the OTA according to the first aspect of the present invention, there are the same advantages as those in the OTA according to the first aspect.

In a preferred embodiment of the OTA according to the second aspect of the present invention, the first I-V converter is formed by first and second serially-connected diodes, the second I-V converter is formed by third and fourth serially-connected diodes, and the third I-V converter is formed by a fifth diode and a fifth bipolar transistor.

The first output current flows through the fifth diode. The second output current flows through the fifth transistor. The third output voltage is given by the sum of a forward voltage drop of the fifth diode and a base-to-emitter voltage of the fifth transistor.

An OTA according to a third aspect of the present invention is comprised of a V-I converter, a first I-V converter, a second I-V converter, a third I-V converter, a quadritail cell of first, second, third, and fourth emitter-coupled bipolar transistors driven by a common constant current.

Emitter areas of the second and third transistors are K_1 times as large as those of the first and fourth transistors, where K_1 is a constant greater than unity.

The V-I converter converts a differential input
5 voltage to first, second, third, and fourth output currents linearly related to the differential input voltage. The third output current is equal to the first output current multiplied by a , where a is a constant. The fourth output current is equal to the second output current multiplied by b ,
10 where b is a constant.

The first I-V converter converts the first output current to a first output voltage which is applied to a base of the fourth transistor. The first I-V converter is formed by serially-connected fifth and sixth bipolar transistors
15 having diode-connections. An emitter area of the sixth transistor is K_2 times as large as that of the fifth transistor, where K_2 is a constant greater than unity.

The second I-V converter converts the second output current to a second output voltage which is applied to a base
20 of the first transistor. The second I-V converter is formed by serially-connected seventh and eighth bipolar transistors having diode-connections. An emitter area of the eighth transistor is K_2 times as large as that of the seventh transistor.

The third I-V converter converts the fourth output current to a third output voltage which is applied to bases of the second and third transistors. The third I-V converter is formed by a ninth and tenth bipolar transistors. The ninth transistor has a diode connection. The third output current flows through the ninth transistor. The fourth output current flows through the tenth transistor. An emitter area of the ninth transistor is K_3 times as large as that of the fifth and seventh transistors, where K_3 is a constant greater than unity. An emitter area of the tenth transistor is K_4 times as large as that of the fifth and seventh transistors, where K_4 is a constant greater than unity.

The third output voltage is given by the sum of a forward voltage drop of the fifth diode and a base-to-emitter voltage of the fifth transistor.

The constants a , b , K_1 , K_2 , K_3 , and K_4 satisfy a relationship of

$$\frac{a b K_2}{K_1 K_3 K_4} = 1$$

20

Collectors of the first and third transistors of the quadritail cell are coupled together to constitute a first output terminal of the OTA. Collectors of the second and fourth transistors of the quadritail cell are coupled

together to constitute a second output terminal of the OTA.

An output of the OTA is differentially derived from the first and second output terminals.

With the OTA according to the third aspect of the present invention, because the configuration of this OTA is substantially the same as the OTA according to the first aspect, there are the same advantages as those in the OTA according to the first aspect.

10

BRIEF DESCRIPTION OF THE DRAWINGS

In order that the present invention may be readily carried into effect, it will now be described with reference to the accompanying drawings.

Fig. 1 is a circuit diagram showing a conventional bipolar translinear multiplier.

Fig. 2 is a circuit diagram showing a bipolar OTA according to a first embodiment of the present invention.

Fig. 3 is a circuit diagram showing a bipolar OTA according to a second embodiment of the present invention.

20 Fig. 4 is a circuit diagram showing a bipolar OTA according to the second embodiment of the present invention, in which the concrete circuit configuration of the V-I converter and the constant current source is illustrated.

Fig. 5 is a circuit diagram showing a bipolar OTA according to a third embodiment of the present invention.

Fig. 6 is a circuit diagram showing a V-I converter used in the OTA according to the third embodiment of the present invention.

Fig. 7 is a circuit diagram showing a V-I converter used in the OTA according to the first embodiment of the present invention.

10 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described below with reference to the drawings attached.

FIRST EMBODIMENT

As shown in Fig. 2, an OTA according to a first embodiment of the present invention is comprised of a V-I converter 1a, a first diode pair 5a of serially connected diodes D1 and D4, a second diode pair 6a of serially connected diodes D2 and D5, a third diode pair 7a of serially connected diodes D3 and D6, a first differential pair 2 of emitter-coupled npn-type bipolar transistors Q1 and Q2, and a second differential pair 4 of emitter-coupled npn-type bipolar transistors Q3 and Q4.

The V-I converter 1a is applied with a differential input voltage V_i and outputs first, second, and third output

currents I_{A1} , I_{A2} , and $(I_{A1} + I_{A2})^{1/2}$, respectively.

An end of the first diode pair 5a is connected to a first output terminal of the V-I converter 1a. Another end of the first diode pair 5a is connected to a reference voltage line applied with a reference voltage V_{REF} .

An end of the second diode pair 6a is connected to a second output terminal of the V-I converter 1a. Another end of the second diode pair 5a is connected to the reference voltage line applied with the reference voltage V_{REF} .

10 An end of the third diode pair 7a is connected to a third output terminal of the V-I converter 1a. Another end of the third diode pair 7a is connected to the reference voltage line applied with the reference voltage V_{REF} .

A power supply voltage may be used as the reference
15 voltage V_{REF} .

The first diode pair 5a serves as a first I-V converter for converting a current flowing through the pair 5a to a first output voltage (i.e., a forward voltage drop) V_1 . The second diode pair 6a serves as a second I-V converter
20 for converting a current flowing through the pair 6a to a second output voltage (i.e., a forward voltage drop) V_2 . The third diode pair 7a serves as a third I-V converter for converting a current flowing through the pair 7a to a third output voltage (i.e., a forward voltage drop) V_3 .

The emitters of the transistors Q1 and Q2 of the first differential pair 2 are connected to a constant current sink (not shown) sinking a constant current I_{B0} . The first differential pair 2 is driven by the constant current I_{B0} .

5 Bases of the transistors Q1 and Q2, which constitute a pair of input terminals of the differential pair 2, are respectively connected to the terminals of the second and third diode pairs 6a and 7a, respectively. The bases of the transistors Q1 and Q2 are applied with a differential input
10 voltage ΔV_1 , where $\Delta V_1 = V_2 - V_3$.

The emitters of the transistors Q3 and Q4 of the second differential pair 4 are connected to a constant current sink (not shown) sinking a constant current I_{B0} . The second differential pair 4 is driven by the constant current
15 I_{B0} .

Bases of the transistors Q3 and Q4, which constitute a pair of input terminals of the differential pair 4, are respectively connected to the terminals of the third and first diode pairs 7a and 5a, respectively. The bases of the
20 transistors Q3 and Q4 are applied with a differential input voltage ΔV_2 , where $\Delta V_2 = V_3 - V_1$.

Collectors of the transistors Q1 and Q3 are coupled together to constitute a first output terminal of the OTA. Collectors of the transistors Q2 and Q4 are coupled together

to constitute a second output terminal of the OTA.

A differential output current ΔI of the OTA according to the first embodiment is derived from the coupled collectors of the transistors Q1 and Q3 and the coupled
5 collectors of the transistors Q2 and Q4, i.e., from the first and second output terminals.

Next, the operation principle of the OTA according to the first embodiment shown in Fig. 2 is explained below.

Supposing that the V-I converter 1 has a linear
10 transfer characteristic, each of the differential output currents I_{A1} and I_{A2} can be expressed as the sum of the constant current ($I_{O\lambda}/2$) that flows the corresponding output terminal of the converter 1 and a variable current ($G_m V_i/2$) proportional to the applied differential input voltage V_i ,
15 where ($G_m/2$) is the transconductance of the converter 11.

Therefore, the differential output currents I_{A1} and I_{A2} of the converter 1 are given by the above equations (3) and (4), respectively.

Because the differential output currents I_{A1} and I_{A2}
20 flow through the diode pairs 15 and 16, respectively, the voltage drops V_1 and V_2 of the diode pairs 5 and 6 are expressed as the above equations (5) and (6), respectively.

The output current $(I_{A1} I_{A2})^{1/2}$ flows through the diode pair 17. Therefore, the voltage drop V_3 of the diode pair 17

is expressed as the following equation (12).

$$\begin{aligned}
V_3 &= 2 V_T \ln \left(\frac{\sqrt{I_{A1} I_{A2}}}{I_S} \right) = 2 V_T \ln \left(\frac{\sqrt{(I_{OA} + G_m V_i)(I_{OA} - G_m V_i)}}{2 I_S} \right) \\
&= 2 V_T \ln \left(\frac{\sqrt{(I_{OA} + G_m V_i)(I_{OA} - G_m V_i)}}{2 I_S} \right) \\
&= V_T \ln \left(\frac{(I_{OA} + G_m V_i)(I_{OA} - G_m V_i)}{2 I_S} \right) \quad (12) \\
&= \frac{1}{2} \left[2 V_T \ln \left(\frac{I_{OA} + G_m V_i}{2 I_S} \right) + 2 V_T \ln \left(\frac{I_{OA} - G_m V_i}{2 I_S} \right) \right] \\
&= \frac{1}{2} (V_1 + V_2)
\end{aligned}$$

5 The equation (12) means that the voltage drop V_3 of the diode pair 17 is equal to a half of the sum of the first and second voltage drops V_1 and V_2 . In other words, the voltage drop V_3 is equal to the middle point voltage of the sum of the voltages drops V_1 and V_2 .

10 Using the above equations (5), (6), and (12), the differential input voltages ΔV_1 and ΔV_2 of the differential pairs 12 and 14 are given by the following equations (13) and (14), respectively.

$$\begin{aligned}
\Delta V_1 &= V_2 - V_3 = V_2 - \frac{V_1 + V_2}{2} = \frac{V_2 - V_1}{2} \\
&= V_T \ln \left(\frac{I_{OA} - G_m V_i}{2 I_{OB}} \right) - V_T \ln \left(\frac{I_{OA} + G_m V_i}{2 I_{OB}} \right) \\
&= V_T \ln \left(\frac{I_{OA} - G_m V_i}{I_{OA} + G_m V_i} \right)
\end{aligned} \tag{13}$$

$$\begin{aligned}
\Delta V_2 &= V_3 - V_1 = \frac{V_1 + V_2}{2} - V_1 = \frac{V_2 - V_1}{2} \\
&= V_T \ln \left(\frac{I_{OA} - G_m V_i}{2 I_{OB}} \right) - V_T \ln \left(\frac{I_{OA} + G_m V_i}{2 I_{OB}} \right) \\
&= V_T \ln \left(\frac{I_{OA} - G_m V_i}{I_{OA} + G_m V_i} \right) = \Delta V_1
\end{aligned} \tag{14}$$

As clearly seen from the that equations (13) and (14),
5 the differential input voltages ΔV_1 and ΔV_2 are equal.

Substituting the equations (13) and (14) into the
above equation (10a) gives the following equation (15).

$$\begin{aligned}
\Delta I &= I_{BO} \left[\tanh \left\{ \ln \left(\frac{I_{OA} - G_m V_i}{I_{OA} + G_m V_i} \right) \right\} + \tanh \left\{ \ln \left(\frac{I_{OA} - G_m V_i}{I_{OA} + G_m V_i} \right) \right\} \right] \\
&= 2 I_{BO} \tanh \left\{ \ln \left(\frac{I_{OA} - G_m V_i}{I_{OA} + G_m V_i} \right) \right\}
\end{aligned} \tag{15}$$

10

As a result, the differential output current ΔI is
expressed as follows:

$$\begin{aligned}
\Delta I &= 2I_{BO} \tanh \left\{ \frac{1}{2} \ln \left(\frac{I_{OA} - G_m V_i}{I_{OA} + G_m V_i} \right) \right\} \\
&= 2I_{BO} \frac{\sinh \left\{ \ln \left(\frac{I_{OA} - G_m V_i}{I_{OA} + G_m V_i} \right) \right\}}{\cosh \left\{ \ln \left(\frac{I_{OA} - G_m V_i}{I_{OA} + G_m V_i} \right) \right\} + 1} \\
&= 2I_{BO} \left[\frac{(I_{OA} - G_m V_i)^2 - (I_{OA} + G_m V_i)^2}{(I_{OA} + G_m V_i) + (I_{OA} - G_m V_i)^2} \right] \\
&= 2I_{BO} \frac{\{(I_{OA} - G_m V_i) + (I_{OA} + G_m V_i)(I_{OA} - G_m V_i) - (I_{OA} + G_m V_i)\}}{\{(I_{OA} + G_m V_i) + (I_{OA} - G_m V_i)\}^2} \\
&= 2I_{BO} \left[\frac{(I_{OA} - G_m V_i) - (I_{OA} + G_m V_i)}{(I_{OA} + G_m V_i) + (I_{OA} - G_m V_i)} \right] \tag{16} \\
&= 2I_{BO} \frac{2G_m V_i}{2I_{OA}} \\
&= 2I_{BO} \left[\frac{G_m V_i}{I_{OA}} \right]
\end{aligned}$$

It is seen from the equation (16) that the differential output current of the OTA shown in Fig. 2 is linearly related to the differential input voltage V_i .

In the above equation (16), the following identity (17) is utilized.

$$\tanh \left(\frac{x}{2} \right) = \frac{\sinh(x)}{\cosh(x) + 1} \tag{17}$$

The above-described calculation method used in the OTA according to the first embodiment has a similarity to the well-known \tanh^{-1} - \tanh transformation where a pair of output
5 currents of a linear V-I converter are (\tanh^{-1}) -converted to generate first and second output voltages, and the difference between the first and second output voltages is applied to a differential circuit for the \tanh conversion in the well-known Gilbert gain cell.

10 However, in this (\tanh^{-1}) - \tanh conversion method, the following identity (18) is utilized.

$$x = \tanh \left\{ \frac{1}{2} \ln \left(\frac{1+x}{1-x} \right) \right\} \quad (18)$$

15 As seen from the identities (17) and (18), x in the identity (17) is equal to a half of x in the identity (18). Therefore, two diodes are serially connected in each of the first, second, and third I-V converters 5a, 6a, and 7a.

 In the OTA according to the first embodiment, a
20 necessary power supply voltage will become higher than that in the (\tanh^{-1}) - \tanh conversion method by the base-to-emitter voltage V_{BE} of a bipolar transistor. However, the offset of the base-to-emitter voltage V_{BE} , which is due to fluctuation

of the transistor characteristic, can be decreased to $(1/2)^{1/2}$ (≈ 0.707). This is because the offset of the base-to-emitter voltage V_{BE} of the two serially-connected diodes is limited within $(2)^{1/2}$ times as much as that of a single diode.

5

SECOND EMBODIMENT

Fig. 3 shows an OTA according to a second embodiment of the present invention.

The OTA according to the second embodiment has the same configuration as the first embodiment shown in Fig. 2 except that a V-I converter 1b producing four output currents and a third I-V converter 7b formed by a diode D3 and an npn-type bipolar transistor Q5 are provided.

Therefore, the explanation about the same configuration is omitted here by attaching the same reference numerals to the same or corresponding parts or elements in Fig. 3 for the sake of simplification of description.

The V-I converter 1b converts the applied differential input voltage V_i to the first, second, third, and fourth differential output currents I_{A1} and I_{A2} and I_{A1} , and I_{A2} . The third and fourth differential output currents I_{A1} and I_{A2} flow through the diode D3 and the transistor Q5, respectively.

The third voltage drop V_3 is equal to the sum of the base-to-emitter voltage of the transistor Q5 and the forward

voltage drop of the diode D3. Therefore, the voltage drop of the third I-V converter 7b is given by the following equation (19) using the above equation (2).

$$\begin{aligned}
 V_3 &= V_T \ln\left(\frac{I_{A1}}{I_S}\right) + V_T \ln\left(\frac{I_{A2}}{I_S}\right) \\
 &= V_T \ln\left(\frac{I_{OA} + G_m V_i}{2I_S}\right) + V_T \ln\left(\frac{I_{OA} - G_m V_i}{2I_S}\right) \\
 &= V_T \ln\left(\frac{(I_{OA} + G_m V_i)(I_{OA} - G_m V_i)}{4I_S^2}\right) \quad (19) \\
 &= \frac{1}{2} \left[2V_T \ln\left(\frac{I_{OA} + G_m V_i}{2I_S}\right) + 2V_T \ln\left(\frac{I_{OA} - G_m V_i}{2I_S}\right) \right] \\
 &= \frac{1}{2} (V_1 + V_2)
 \end{aligned}$$

The voltage drop V_3 of the third I-V converter 7b is equal to a half of the sum of the first and second voltage drops V_1 and V_2 . As a result, there are the same advantages as those in the first embodiment.

The linear V-I converter 1b is, for example, realized by a circuit configuration as shown in Fig. 4. The constant currents I_{B0} for driving the first and second differential pairs 2 and 4 are simply realized by a current mirror circuit as shown in Fig. 4.

In Fig. 4, npn-type bipolar transistors Q6 and Q7 constitute a differential pair, and npn-type bipolar transistors Q8 and Q9 constitute another differential pair.

The transistors Q6, Q7, Q8, and Q9 have emitter resistors R1, R2, R3, and R4, respectively. The emitters of the transistors Q6 and Q7 are coupled together through the emitter resistors R1 and R2. The emitters of the transistors Q8 and Q9 are
5 coupled together through the emitter resistors R3 and R4.

The connection point of the resistors R1 and R2 is connected to one terminal of a constant current sink C1 sinking a constant current $I_{O\lambda}$. The other terminal of the constant current sink C1 is connected to the ground.

10 The connection point of the resistors R3 and R4 is connected to one terminal of a constant current sink C2 sinking a constant current $I_{O\lambda}$. The other terminal of the constant current sink C2 is connected to the ground.

The differential input voltage V_i is applied across
15 the bases of the transistors Q6 and Q7 and across the bases of the transistors Q8 and Q9.

Collectors of the transistors Q6, Q7, Q8, and Q9 are connected to the diode pair 5a, the diode pair 6a, the diode D3, and the transistor Q5.

20 An anode of a diode D7 is connected to the cathodes of the diodes D1, D2, and D3, and the collector of the transistor Q5. A cathode of the diode D7 is connected to a power supply line applied with a power supply voltage V_{CC} . The diode D7 serves to define the reference voltage V_{REF} .

The V-I converter 1b with the configuration shown in Fig. 4 does not have a complete linearity. However, it realizes a practically linear V-I converter characteristic with a simplified configuration.

5 The current mirror circuit 3 is comprised of npn-type bipolar transistors Q10, Q11, and Q12 whose emitters are connected in common to the ground, and a current source C3 supplying an constant current I_{E0} . Bases of the transistors Q10, Q11, and Q12 are coupled together. The bases of the
10 transistors Q11 and Q12 are connected to the coupled emitters of the transistors Q1 and Q2 and the coupled emitters of the transistors Q3 and Q4, respectively. The base and a collector of the transistor Q10 are coupled together to be connected to the current source C3.

15 A load resistor R5 is connected between the coupled collectors of the transistors Q1 and Q3 and the power supply voltage V_{cc} . Another load resistor R6 is connected between the coupled collectors of the transistors Q2 and Q4 and the power supply voltage V_{cc} .

20 A differential output voltage ΔV_o of the OTA is derived from the load resistors R6.

THIRD EMBODIMENT

Fig. 5 shows an OTA according to a third embodiment of the present invention.

The OTA according to the third embodiment is comprised of a V-I converter 1c, a first I-V converter 5b, a second I-V converter 6b, a third I-V converter 7c, and a quadritail cell 8.

5 The V-I converter 1c is applied with the differential input voltage V_i and outputs first, second, third, and fourth output currents I_{A1} , I_{A2} , aI_{A1} , and bI_{A2} , respectively, where a and b are constants.

10 The first I-V converter 5b converts the first output current I_{A1} to a first output voltage, which is applied to a base of the transistor Q4. The first I-V converter 5b is formed by serially-connected npn-type bipolar transistors Q13 and Q14 having diode-connections. An emitter area of the transistor Q14 is K_2 times as large as that of the transistor
15 Q13, where K_2 is a constant greater than unity.

 The second I-V converter 6b converts the second output current I_{A2} to a second output voltage, which is applied to a base of the transistor Q1. The second I-V converter 6b is formed by serially-connected npn-type bipolar
20 transistors Q15 and Q16 having diode-connections. An emitter area of the transistor Q16 is K_2 times as large as that of the transistor Q15.

 The third I-V converter 7c converts the output current aI_{A1} to a third output voltage, which is applied to

bases of the transistors Q2 and Q3. The third I-V converter 7c is formed by npn-type bipolar transistors Q17 and Q18. The transistor Q17 has a diode connection. The third output current aI_{A1} flows through the transistor Q17. The fourth
5 output current bI_{A2} flows through the transistor Q16. An emitter area of the transistor Q17 is K_3 times as large as that of the transistors Q13 and Q15, where K_3 is a constant greater than unity. An emitter area of the transistor Q18 is K_4 times as large as that of the transistors Q13 and Q15,
10 where K_4 is a constant greater than unity.

The third output voltage V_3 is given by the sum of a forward voltage drop of the diode Q17 and a base-to-emitter voltage of the transistor Q18.

Collectors of the transistors Q1 and Q3 of the
15 quadritail cell 8 are coupled together to constitute a first output terminal of the OTA. Collectors of the transistors Q2 and Q4 of the quadritail cell 8 are coupled together to constitute a second output terminal of the OTA.

An output of the OTA is differentially derived from
20 the first and second output terminals.

Next, the operation principle of the OTA according to the third embodiment shown in Fig. 5 is explained below.

In Fig. 5, if collector currents of the transistors Q1, Q2, Q3, and Q4 of the quadritail cell 8 are defined as

I_{C1} , I_{C2} , I_{C3} , and I_{C4} , respectively, they are expressed as the following equations, (20), (21), (22), and (23) by using the above equation (1'), respectively,

$$5 \quad I_{C1} = I_S \exp\left(\frac{V_{B1} - V_E}{V_T}\right) \quad (20)$$

$$I_{C2} = K_1 I_S \exp\left(\frac{V_{B2} - V_E}{V_T}\right) \quad (21)$$

$$I_{C3} = K_1 I_S \exp\left(\frac{V_{B3} - V_E}{V_T}\right) = I_{C2} \quad (22)$$

$$I_{C4} = I_S \exp\left(\frac{V_{B4} - V_E}{V_T}\right) \quad (23)$$

10 where V_E is the common emitter voltage of the transistors Q1, Q2, Q3, and Q4 and V_{B1} , V_{B2} , V_{B3} , and V_{B4} are base voltages thereof, respectively.

Also, the quadritail cell 8 is driven by a single tail current I_{B0} and therefore, the following equation (24)
15 is established,

$$I_{C1} + I_{C2} + I_{C3} + I_{C4} = I_{B0} \quad (24)$$

where $I_{C2} = I_{C3}$.

20 Solving the equations (20) to (24) gives the following equation (25).

$$I_S \exp\left(\frac{V_E}{V_T}\right) = \frac{I_{BO}}{\exp\left(\frac{V_{B1}}{V_T}\right) + 2K_1 \exp\left(\frac{V_{B2}}{V_T}\right) + \exp\left(\frac{V_{B4}}{V_T}\right)} \quad (25)$$

Accordingly, the differential output current ΔI of
5 the OTA shown in Fig. 5 is expressed as follows.

$$\begin{aligned} \Delta I &= I_{01} - I_{02} \\ &= \frac{I_{BO} \left\{ \exp\left(\frac{V_{B1}}{V_T}\right) - \exp\left(\frac{V_{B4}}{V_T}\right) \right\}}{\exp\left(\frac{V_{B1}}{V_T}\right) + 2K_1 \exp\left(\frac{V_{B2}}{V_T}\right) + \exp\left(\frac{V_{B4}}{V_T}\right)} \end{aligned} \quad (26)$$

If the V-I converter 1c is linearly related to the
10 differential input voltage V_i , the output currents I_{A1} and I_{A2}
are expressed by the above equations (3) and (4).

Accordingly, the base voltages V_{B1} , V_{B2} , V_{B3} , and V_{B4} of
the transistors Q1, Q2, Q3, and Q4 of the quadritail cell 8
are expressed by the following equations (27), (28), and (29),
15 respectively.

$$\begin{aligned} V_{B1} &= V_{CC} - V_T \ln\left(\frac{I_{OA} - G_m V_i}{I_S}\right) - V_T \ln\left(\frac{I_{OA} - G_m V_i}{K_2 I_S}\right) \\ &= V_{CC} - V_T \ln\left\{ \frac{(I_{OA} - G_m V_i)(I_{OA} - G_m V_i)}{K_2 I_S^2} \right\} \end{aligned} \quad (27)$$

$$\begin{aligned}
V_{B2} = V_{B3} = V_{CC} - V_T \ln \left\{ \frac{a(I_{OA} + G_m V_i)}{K_3 I_S} \right\} - V_T \ln \left\{ \frac{b(I_{OA} - G_m V_i)}{K_4 I_S} \right\} \\
= V_{CC} - V_T \ln \left\{ \frac{ab(I_{OA} + G_m V_i)(I_{OA} - G_m V_i)}{K_3 K_4 I_S^2} \right\}
\end{aligned} \tag{28}$$

$$\begin{aligned}
V_{B4} = V_{CC} - V_T \ln \left(\frac{I_{OA} + G_m V_i}{I_S} \right) - V_T \ln \left(\frac{I_{OA} + G_m V_i}{K_2 I_S} \right) \\
= V_{CC} - V_T \ln \left\{ \frac{(I_{OA} + G_m V_i)(I_{OA} + G_m V_i)}{K_2 I_S^2} \right\}
\end{aligned} \tag{29}$$

5 Substituting the equations (27), (28), and (29) into (26) gives the following equation (30a).

$$\begin{aligned}
\Delta I = I_{BO} \times \\
\frac{(I_{OA} + G_m V_i)(I_{OA} + G_m V_i) - (I_{OA} - G_m V_i)(I_{OA} - G_m V_i)}{(I_{OA} + G_m V_i)(I_{OA} + G_m V_i) - (I_{OA} - G_m V_i)(I_{OA} - G_m V_i) + \frac{2K_1 K_3 K_4}{ab K_2} (I_{OA} + G_m V_i)(I_{OA} - G_m V_i)}
\end{aligned} \tag{30a}$$

10

To equalize the equation (30a) to the form of the above equation (16), the following relationship (30b) needs to be satisfied.

$$\begin{aligned}
\Delta I = I_{BO} \frac{\{(I_{OA} + G_m V_i) + (I_{OA} + G_m V_i)\} \{(I_{OA} - G_m V_i) - (I_{OA} - G_m V_i)\}}{\{(I_{OA} + G_m V_i)(I_{OA} + G_m V_i) + (I_{OA} - G_m V_i)(I_{OA} - G_m V_i)\}^2} \\
= I_{BO} \frac{(I_{OA} + G_m V_i) - (I_{OA} - G_m V_i)}{(I_{OA} + G_m V_i) + (I_{OA} - G_m V_i)}
\end{aligned} \tag{30b}$$

15

Accordingly, the following relationship (30c) needs to be established.

5
$$\frac{2K_1 K_3 K_4}{a b K_2} = 2 \quad (30c)$$

As a result, the following relationship (31) needs to be satisfied.

10
$$\frac{a b K_2}{K_1 K_3 K_4} = 1 \quad (31)$$

When the relationship (31) is satisfied, the differential output current ΔI is expressed as follows.

15
$$\Delta I = \frac{I_{BO} G_m V_i}{I_{OA}} \quad (32)$$

As seen from the expression (32), the output current ΔI of the OTA according to the third embodiment is linearly related to the differential input voltage V_i .

20 The V-I converter 1c used in the third embodiment is, for example, realized by a circuit configuration shown in Fig. 6. This circuit configuration is substantially the same as the known OTA which was developed by the inventor, Kimura,

and was disclosed in the Japanese Non-Examined Patent Publication No. 9-238032 published in September 1997, and in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, Part I, Vol. 45, No. 1, pp. 108-113, January 1998.

5 As shown in Fig. 6, this V-I converter 1c includes a balanced differential pair of npn bipolar transistors Q31 and Q32 whose emitter areas are equal to each other.

 Emitters of the transistors Q31 and Q32 are coupled together through an emitter resistor R31 having a resistance
10 R. The emitter of the transistor Q31 is further connected to the ground through an emitter-follower-augmented current mirror circuit 31. The emitter of the transistor Q32 is further connected to the ground through an emitter-follower-augmented current mirror circuit 32.

15 The current mirror circuits 31 and 32 serve as active loads of the transistors Q31 and Q32, respectively. Output currents I_{A1} and aI_{A1} , and I_{A2} and bI_{A2} of the V-I converter 1c are derived from the current mirrors 31 and 32, respectively.

 A collector of the transistor Q31 is applied with a
20 power supply voltage V_{CC} through a constant current source C31 supplying a constant current I_{OA} . The transistor Q31 is driven by the constant current I_{OA} .

 A collector of the transistor Q32 is applied with the same power supply voltage V_{CC} through a constant current

source C32 supplying the same constant current I_{OA} . The transistor Q32 is driven by the constant current I_{OA} .

The differential input voltage V_i is applied across bases of the transistor Q31 and Q32. A current i will flow
5 through the emitter resistor R31 according to the value of the applied differential input voltage V_i .

With the V-I converter 1c shown in Fig. 6, since the transistors Q31 and Q32 are driven by the same constant current I_{OA} , the base-to-emitter voltages V_{BE31} and V_{BE32} are
10 equal to each other. Therefore, the following equation (33) is established.

$$V_i = R i \quad (33)$$

15 Accordingly, the current i is expressed as

$$i = \frac{V_i}{R} \quad (34)$$

Thus, the output currents I_{A1} and I_{A2} outputted from
20 the current mirror circuits 31 and 32 are given by the following expressions (35a) and (35), respectively.

$$I_{A1} = I_{0A} + i = I_{0A} + \frac{V_i}{R} \quad (35a)$$

$$I_{A2} = I_{0A} - i = I_{0A} - \frac{V_i}{R} \quad (35b)$$

The current mirror circuit 31 is comprised of three
 5 npn bipolar transistors Q33, Q34 and Q46 whose bases are
 coupled together, an npn bipolar transistor Q35 serving as an
 emitter-follower transistor, and a constant voltage source
 V31 supplying a constant voltage V_{Ls} . The transistor Q46 has
 an emitter area b times as large as that of the transistors
 10 Q33 and Q34.

A collector of the transistor Q33 is connected to the
 emitter of the transistor Q31. An emitter of the transistor
 Q33 is connected to the ground. The coupled bases of the
 transistors Q33, Q34, and Q46 are connected to a negative
 15 electrode of the voltage source V33. An emitter of the
 transistor Q34 is connected to the ground. A base of the
 transistor Q35 is connected to the collector of the
 transistor Q31. A collector of the transistor Q35 is applied
 with the power supply voltage V_{cc} . An emitter of the
 20 transistor Q35 is connected to the positive electrode of the
 voltage source V31.

The output current $I_{A2} = I_{0A} - (V_i/R)$ is derived from
 a collector of the transistor Q34. The output current bI_{A2} is

derived from a collector of the transistor Q46.

The constant voltage source V31 serves to shift the voltage level at the coupled bases of the transistors Q33, Q34, and Q46.

5 Similarly, the current mirror 32 is comprised of three npn bipolar transistors Q36, Q37, and Q47 whose bases are coupled together, an npn bipolar transistor Q38 serving as an emitter-follower transistor, and a constant voltage source V32 supplying the same constant voltage V_{Ls} as that of
10 the voltage source V31. The transistor Q47 has an emitter area a times as large as that of the transistors Q36 and Q37.

A collector of the transistor Q36 is connected to the emitter of the transistor Q32. An emitter of the transistor Q36 is connected to the ground. The coupled bases of the
15 transistors Q36 and Q37 are connected to a negative electrode of the voltage source V32. An emitter of the transistor Q37 is connected to the ground. A base of the transistor Q38 is connected to the collector of the transistor Q32. A collector of the transistor Q38 is applied with the power supply
20 voltage V_{cc} . An emitter of the transistor Q38 is connected to the positive electrode of the voltage source V32.

The output current $I_{A1} = I_0 + (V_1/R)$ is derived from a collector of the transistor Q34. The output current aI_{A1} is derived from a collector of the transistor Q47.

The constant voltage source V32 serves to shift the voltage level at the coupled bases of the transistors Q36, Q37, and Q47.

As clearly seen from the equations (35a) and (35b),
5 the V-I converter 1c shown in Fig. 6 has a completely or perfectly linear operation.

Fig. 7 shows an example of the V-I converter 1a used for the OTA according to the first embodiment shown in Fig. 2.

This circuit configuration corresponds to a
10 configuration obtained by adding pnp-type bipolar transistors Q39 and Q40 and npn-type bipolar transistors Q41, Q42, Q43, Q44, Q45 to the above V-I converter 1c shown in Fig. 6, except that the bipolar transistors Q46 and Q47 are omitted.

As shown in Fig. 7, the transistors Q39 and Q40
15 constitute a current mirror circuit. Bases of the transistors Q39 and Q40 are coupled together. Emitters of the transistors Q39 and Q40 are applied with the power supply voltage V_{cc} . The base and a collector of the transistor Q39 are coupled together. The collector of the transistor Q39 is connected to
20 the collector of the transistor Q37. The reference current I_{A1} from the transistor Q37 is supplied to the collector of the transistor Q39, and a mirror current I_{A1} is outputted from a collector of the transistor Q40.

The transistors Q41 and Q43 constitute a current mirror circuit. Emitters of the transistors Q41 and Q43 are connected to the ground. Base of the transistors Q41 and Q43 are connected in common to the collector of the transistor Q34. A collector of the transistor Q41 is connected to the collector of the transistor Q40. The reference current I_{A1} from the transistor Q40 is supplied to the collector of the transistor Q41, and a mirror current I_{A1} is outputted from a collector of the transistor Q43.

Base of the transistors Q42 and Q44 are connected in common to the collector of the transistor Q40. An emitter of the transistor Q42 is connected to the bases of the transistors Q41 and Q43 and the collector of the transistor Q34. An emitter of the transistor Q44 is connected to a collector and a base of the transistor Q45. The base and collector of the transistor Q45 are coupled together. An emitter of the transistor Q45 is connected to the ground.

The current I_{A2} from the collector of the transistor Q34 is outputted from a collector of the transistor Q42.

The current $(I_{A1} I_{A2})^{1/2}$ is outputted from a collector of the transistor Q44. The reason is as follows:

If base-to-emitter voltages of the transistors Q41, Q42, Q44, and Q45 are defined as V_{BE41} , V_{BE42} , V_{BE44} , and V_{BE45} , respectively, the base-to-emitter voltages V_{BE41} , V_{BE42} , V_{BE44} ,

and V_{BE45} are expressed in the following equations (36), (37), and (38), using the above-identified equation (2).

$$V_{BE41} = V_T \ln\left(\frac{I_{A1}}{I_S}\right) \quad (36)$$

5 $V_{BE42} = V_T \ln\left(\frac{I_{A2}}{I_S}\right) \quad (37)$

$$V_{BE44} = V_{BE45} = V_T \ln\left(\frac{I_{OUT}}{I_S}\right) \quad (38)$$

On the other hand, since the bases of the transistors Q42 and Q44 are coupled together and the emitters of the
10 transistors Q41 and Q45 are connected to the ground, the following equation (39) is established among the base-to-emitter voltages V_{BE41} , V_{BE42} , V_{BE44} , and V_{BE45} .

$$V_{BE41} + V_{BE42} = V_{BE44} + V_{BE45} \quad (39)$$

15

Substituting the (36), (37), and (38) into the equation (39) give the following equation (40).

$$I_{OUT}^2 = I_{A1} \cdot I_{A2} \quad (40)$$

20

As a result, the following equation (41) is obtained.

$$I_{OUT} = \sqrt{I_{A1} \cdot I_{A2}} \quad (41)$$

5 Thus, the output current I_{OUT} is proportional to the square root of the product of the currents I_{A1} and I_{A2} .

 While the preferred forms of the present invention have been described, it is to be understood that modifications will be apparent to those skilled in the art
10 without departing from the spirit of the invention. The scope of the invention, therefore, is to be determined solely by the following claims.

 Each feature disclosed in this specification (which term includes the claims) and/or shown in the drawings may be incorporated in the invention independently of other disclosed and/or illustrated features.

 The description of the invention with reference to the drawings is by way of example only.

What is claimed is:

1. A bipolar operational transconductance amplifier comprising:

5 (a) a V-I converter for converting a differential input voltage to first and second output currents linearly related to a differential input voltage and for generating a third output current;

(b) a first I-V converter for converting said first
10 output current to a first output voltage;

(c) a second I-V converter for converting said second output current to a second output voltage;

(d) a third I-V converter for converting said third output current to a third output voltage;

15 said third output voltage being equal to a middle point voltage of a sum of said first and second output voltages;

(e) a first differential pair of first and second emitter-coupled bipolar transistors driven by a first
20 constant current; and

(f) a second differential pair of third and fourth emitter-coupled bipolar transistors driven by a second constant current;

wherein said first output voltage is applied to a base of said fourth transistor, said second output voltage is applied to a base of said first transistor, and said third output voltage is commonly applied to bases of said second and third transistors;

wherein collectors of said first and third transistors of said first differential pair are coupled together to constitute a first output terminal of said OTA;

and wherein collectors of said second and fourth transistors of said second differential pair are coupled together to constitute a second output terminal of said OTA;

and wherein an output of said OTA is differentially derived from said first and second output terminals.

2. An amplifier as claimed in claim 1, wherein said third output current of said third I-V converter is proportional to a square root of a product of said first and second output currents of said V-I converter.

3. An amplifier as claimed in claim 1, wherein each of said first, second, and third I-V converters is formed by two serially-connected diodes.

4. An amplifier as claimed in claim 1, wherein each of said diodes is formed by a bipolar transistor whose base and collector are coupled together.

5 5. An operational transconductance amplifier comprising:

(a) a V-I converter for converting a differential input voltage to first, second, third, and fourth output currents linearly related to a differential input voltage;

(b) a first I-V converter for converting said first
10 output current to a first output voltage;

(c) a second I-V converter for converting said second output current to a second output voltage;

(d) a third I-V converter for converting said third
output current to a third output voltage;

15 said third output voltage being equal to a middle point voltage of a sum of said first and second output voltages;

(e) a first differential pair of first and second emitter-coupled bipolar transistors driven by a first
20 constant current; and

(f) a second differential pair of third and fourth emitter-coupled bipolar transistors driven by a second constant current;

wherein said first output voltage is applied to a base of said fourth transistor, said second output voltage is applied to a base of said first transistor, and said third output voltage is applied to bases of said second and third transistors;

and wherein collectors of said first and third transistors of said first differential pair are coupled together to constitute a first output terminal of said OTA;

and wherein collectors of said second and fourth transistors of said second differential pair are coupled together to constitute a second output terminal of said OTA;

and wherein an output of said OTA is differentially derived from said first and second output terminals.

6. An amplifier as claimed in claim 5, wherein said first I-V converter is formed by first and second serially-connected diodes, said second I-V converter is formed by third and fourth serially-connected diodes, and said third I-V converter is formed by a fifth diode and a fifth bipolar transistor;

and wherein said first output current flows through said fifth diode, said second output current flows through said fifth transistor, and said third output voltage is given by a sum of a forward voltage drop of said fifth diode and a

base-to-emitter voltage of said fifth transistor.

7. An operational transconductance amplifier comprising:

(a) a V-I converter for converting a differential input
5 voltage to first, second, third, and fourth output currents
linearly related to said differential input voltage;

said third output current being equal to said first
output current multiplied by a , where a is a constant;

said fourth output current being equal to said first
10 output current multiplied by b , where b is a constant;

(b) a first I-V converter for converting said first
output current to a first output voltage;

said first I-V converter being formed by serially-
connected fifth and sixth bipolar transistors having diode-
15 connections;

an emitter area of said sixth transistor being K_2
times as large as that of said fifth transistor, where K_2 is
a constant greater than unity;

(c) a second I-V converter for converting said second
20 output current to a second output voltage;

said second I-V converter being formed by serially-
connected seventh and eighth bipolar transistors having
diode-connections;

an emitter area of said eighth transistor being K_2 times as large as that of said seventh transistor;

(d) a third I-V converter for converting said third output current to a third output voltage;

5 said third I-V converter being formed by a ninth and tenth bipolar transistors;

 said ninth transistor having a diode connection;

 said third output current flowing through said ninth transistor;

10 said fourth output current flowing through said tenth transistor;

 an emitter area of said ninth transistor being K_3 times as large as that of said fifth and seventh transistors, where K_3 is a constant greater than unity;

15 an emitter area of said tenth transistor being K_4 times as large as that of said fifth and seventh transistors, where K_4 is a constant greater than unity;

 said third output voltage being given by a sum of a forward voltage drop of said fifth diode and a base-to-emitter voltage of said fifth transistor;

20 (e) a quadritail cell of first, second, third, and fourth emitter-coupled bipolar transistors driven by a common constant current;

emitter areas of said second and third transistors being K_1 times as large as those of said first and fourth transistors, where K_1 is a constant greater than unity;

wherein said first output voltage is applied to a base of said fourth transistor, said second output voltage is applied to a base of said first transistor; said third output voltage is commonly applied to bases of said second and third transistors;

and wherein collectors of said first and third transistors of said quadritail cell are coupled together to constitute a first output terminal of said OTA, and collectors of said second and fourth transistors of said quadritail cell are coupled together to constitute a second output terminal of said OTA;

and wherein said constants a , b , K_1 , K_2 , K_3 , and K_4 satisfy a relationship of

$$\frac{a b K_2}{K_1 K_3 K_4} = 1$$

and wherein an output of said OTA is differentially derived from said first and second output terminals.



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Claims searched: 1-7

Examiner: D. Midgley
Date of search: 10 July 1998

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Search Report under Section 17

Databases searched:

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UK C1 (Ed.P): H3W WUL, WVP

Int C1 (Ed.6): G06G 7/163 H03F 1/32, 3/45

Other: ONLINE: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	US 5331289 (TEKTRONICS)	1,5,7

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